

## IN THE SPECIFICATION

Please amend the paragraph 0039 as follows:

*Ar*  
*Not id*  
*NaCesary item*

-- FIG. 1 illustrates a first step 11 of a semiconductor fabrication process, in accordance with a preferred embodiment of the present invention. First step 11 indicates a poly deposition layer 14 located above STI 16 and 18. A TEOS deposition layer 12 is situated above poly deposition layer 14. Finally, an SiN deposition layer 10 is situated above TEOS deposition layer 12. Note that the acronym "TEOS," as utilized herein, refers to "Tetraethoxysilane." For brevity, however, the term TEOS will be utilized primarily herein. ~~Thus, first step 11 of FIG. 1 indicates the formation of a gate oxide.~~ Thus, as indicated in first step 11, DRAM poly gate patterning may be performed utilizing a hard mask. Note that in FIGS. 1 to 15 herein, analogous parts are indicated by identical reference numerals. Thus, FIGS. 1 to 15 together represent a semiconductor fabrication process that may be implemented in accordance with a preferred or alternative embodiments of the present invention. --

Please amend paragraph 0040 as follows:

*A3*

-- FIG. 2 illustrates a second step 13 of the semiconductor fabrication process disclosed herein, in accordance with a preferred embodiment of the present invention. In second step 13, a poly gate can be is defined (i.e., a DRAM gate is defined). Additionally, a cell LDD implant step can be is performed as part of second step 13 as indicated by the formation of resists 20-32, which can assist in the formation of a drain or drain feature. Note that the acronym LDD, which is utilized herein, refers to the term "Lightly Doped Drain." The term "LDD" is well known in the semiconductor fabrication arts. --

*Appl. No. 09/975,840*

Please amend the paragraph 0046 as follows:

*Appl. No. 09/975,840*

-- FIG. 13 depicts a thirteenth step 35 of the semiconductor fabrication process disclosed herein, in accordance with a preferred embodiment of the present invention. As indicated in FIG. 13, ~~a~~ an RPO photo and etch step can be performed, resulting in Co-Salicide formation. Co-Salicide 90 is illustrated in FIG. 13. Additionally, a SiN spacer 92 is depicted. --

*Appl. No. 09/975,840*

Please amend the paragraph 0050 as follows:

*Appl. No. 09/975,840*

-- FIG. 17 depicts a flow of operations 101 illustrating continued operational steps that may be followed to implement a preferred embodiment of the present invention. Note that the operations depicted in FIG. 17 represent continued operational steps that are described herein with reference to FIG. 16. Thus, the operation illustrated at block 112 of FIG. 17 can be processed immediately following the operation depicted at block 110. As indicated at block 112, a spacer TEOS dry etch may be performed with a stop on a SiN layer (e.g., see FIG. 9), and followed thereafter by an extra photo mask to open the DRAM array. A wet dip can be utilized to remove the spacer TEOS (e.g., see FIG. 10). After a resist stripper operation is performed, as illustrated at block 114, a SiN dry etch with a stop on TEOS can be processed. A wet dip may then be utilized to remove the space TEOS (e.g., see FIG. 11). Then, as illustrated at block 116, ~~an RPO is defined and~~ Co-Salicide formation takes place (e.g., see FIG. 13). Finally, as illustrated at block 118 standard logical processes may occur using an MIM capacitor formed between a metal one and metal two layer, as a result of the processing of the semiconductor fabrication steps described herein. --

**IN THE TITLE**

Please cancel the original title of "Compatible Embedded DRAM Process for MIM Capacitor" and replace with the following new title: "Methods and Systems for Forming Embedded DRAM for an MIM Capacitor"